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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,218	12/28/2001	Clarence Rick Thompson	1662-49900 (P98-2426)	7771

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EXAMINER	
MATTHEW, AARON D	
ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,218	THOMPSON ET AL.	
	Examiner	Art Unit	
	Aaron D Matthew	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/10/02,9/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:
    - The word, "experience", on line 3 of par. 0013, should be replaced with, "experienced";
    - The phrase, "without the involvement of external controlling logic such as the host processor," on lines 4-5 of par. 0013, is somewhat unclear; the examiner suggests changing the phrase to read, "without the involvement of external controlling logic such as host processor controlling logic";

    Appropriate correction is required.

Claim Objections

2. Claims 1-21 have been examined.
3. Claims 5-7, and 14-15 are objected to because of the following informalities:
    - The word, "process", on line 2 of claim 5 and line 1 of claim 14, should be changed to read, "processor;"
    - To avoid confusion, the examiner suggests including the word, "fan", before the reference to "controller" on line 2 of claim 6, and line 2 of claim 7;

    Appropriate correction is required.

Claim 15 is objected to based on its dependence on claim 14.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "said register" in line 1. As claim 7 is dependent upon claim 1, and a register is not disclosed until claim 5, there is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 8, 10-13, 17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair, (US 6,318,965 B1), and further in view of Sekiguchi, (US 6,398,505 B1).

Regarding claim 1, Nair teaches a computer system comprising:

- A host processor, (see Fig. 2, element 62);
- A plurality of fan controllers coupled to said host processor, (see Fig. 2, elements 56 and 57); and
- A fan coupled to each fan controller, (see Fig. 2, elements 76 and 60);

Nair fails to teach that said fan controllers are inter-connected by a fault signal which is used to transmit fault information between the fan controllers without host processor involvement. However, Nair does teach a need for a fan which can interface directly with one or more fans to optimize fan performance, (see col. 1, lines 55-60).

Sekiguchi teaches a cooling apparatus for use in a computer system, comprising a plurality of fan controllers, wherein the fan controllers are inter-connected by a fault signal that is used to transmit fault information between the fan controllers, (see col. 4, lines 15-20, col. 6, lines 59-67, and col. 8, lines 40-49), without host processor involvement, (note that "monitoring portion 5", of Fig. 2, is independent of a host processor).

Sekiguchi and Nair are analogous art because they are from the same field of endeavor, viz., the operation of fan controllers in a computer system.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair, in order to achieve a cooling system in a system comprising a host processor, in which a plurality of fan controllers are capable of relaying fault information without host processor involvement.

One of ordinary skill in the art would have been motivated to combine the teachings because the cooling system of Sekiguchi offers distinct advantages over the teachings of Nair. Note col. 13, lines 35-39, of Sekiguchi, which disclose that the independence of each of the plurality of the fan controllers taught therein reduces maintenance costs in the cooling system. Also, by enabling fault signal communication between the independent fan controllers, the overall cooling power of the system is not necessarily reduced as a result of failure of a single fan unit, (see col. 4, lines 38-47). Therefore, one of ordinary skill in the art would have been clearly motivated to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair in order to prevent loss of overall cooling power in the event of a fan failure, and to reduce maintenance costs resulting from said failure.

Regarding claim 10, Nair discloses a fan controller comprising:

- An interface to controlling logic, (see col. 2, lines 30-35);
- An interface to a fan which permits said fan controller to control the speed of said fan, (see col. 2, lines 40-50); and
- A programmable register accessible by a host processor via said controlling logic, (see col. 3, lines 34-38);

Nair fails to disclose that said fan controller also comprises an input/output fault signal adapted to be coupled to another fan controller through which fault information can be shared between fan controllers without host processor involvement. However, Nair does teach a need for a fan which can interface directly with one or more fans to optimize fan performance, (see col. 1, lines 55-60).

Sekiguchi teaches a cooling apparatus for use in a computer system, comprising a plurality of fan controllers, wherein the fan controllers are inter-connected by an input/output fault signal that is used to transmit fault information between the fan controllers, (see col. 4, lines 15-20, col. 6, lines 59-67, and col. 8, lines 40-49), without host processor involvement, (note that "monitoring portion 5", of Fig. 2, is independent of a host processor).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair, in order to achieve a cooling system in a system comprising a host processor, in which a plurality of fan controllers are capable of relaying fault information without host processor involvement.

One of ordinary skill in the art would have been motivated to combine the teachings because the cooling system of Sekiguchi offers distinct advantages over the teachings of Nair. Note col. 13, lines 35-39, of Sekiguchi, which disclose that the independence of each of the plurality of the fan controllers taught therein reduces maintenance costs in the cooling system. Also, by enabling fault signal communication between the independent fan controllers, the overall cooling power of the system is not necessarily reduced as a result of failure of a single fan unit, (see col. 4, lines 38-47). Therefore, one of ordinary skill in the art would have been clearly motivated to combine the intercommunicating fan controllers of Sekiguchi with the computer cooling system of Nair in order to prevent loss of overall cooling power in the event of a fan failure, and to reduce maintenance costs resulting from said failure.

Regarding claims 2, 3, 11 and 12, note that Sekiguchi teaches that when a fault signal, indicating a fan fault condition, is sent from one fan controller, another fan

controller receives the fault signal and responds by increasing the speed of its fan, (see col. 2, lines 27-35).

Regarding claims 4 and 13, see Sekiguchi, Fig. 2, element 5, wherein the monitoring portion functions as a bridge.

Regarding claims 8 and 17, see Sekiguchi, col. 6, lines 59-67.

Claims 19-21 are rejected because they recite limitations similar to claims 1-3, except in the context of a method of controlling fans in a computer system. Please see the discussion regarding claims 1-3.

6. Claims 5, 9, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair, in view of Sekiguchi, as applied to claims 1 and 10 above, and further in view of White, (US 2002/0010881 A1).

Regarding claims 5 and 14, Nair, in view of Sekiguchi, fails to teach that each fan controller includes a register which said host processor can access to determine which fan controller asserted said fault signal. However, note Nair, col. 4, lines 1-6, wherein each fan controller includes non-volatile memory for storing alarm information.

White teaches a computer system comprising a cooling fan, in which a fan unit comprises a register, (see par. 0077), which the host processor can access to determine whether the fan unit has assert a fault signal, (see par. 0082, and note lines 4-6).

White, Nair and Sekiguchi are analogous art because they are from the same field of endeavor, viz., cooling apparatus control in computer systems.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fan unit register field of White, with the fan controller system of Nair, in view of Sekiguchi, in order to improve the host processors ability to monitor the functions of the fan controllers in the event of a cooling system failure.

One of ordinary skill in the art would have been motivated to combine the teachings because the register disclosed in White provides a distinct advantage to the cooling system of Nair, in view of Sekiguchi. Nair teaches that the host processor should have the greatest knowledge of the thermal load of the system, (see col. 3, lines 20-25). As such, one of ordinary skill in the art would have clearly recognized that the host processor must be fully cognizant of the source of any errors encountered in the cooling system. Therefore, there is a clearly represented need for the host

processor of Nair to be able to determine the source of a fan fault signal transmitted in the system of Nair, in view of Sekiguchi. The register of White provides an easily transferable means of utilizing the non-volatile memory, disclosed on col. 4, lines 1-6 of Nair, to provide fault source information to the host processor. One of ordinary skill in the art would have been motivated to combine the register of White with the non-volatile memory of Nair in order to enable host processor access to fault source information.

Regarding claims 9 and 18, see par. 0082 of White, wherein the register comprises a fan speed value.

7. Claims 6, 7, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair, in view of Sekiguchi and White, as applied to claims 5 and 14 above, and further in view of Beeghly, (US 4,336,463).

Regarding claims 6, 7 and 15, Nair, in view of Sekiguchi and White, fails to disclose that said register also includes bits which can be set by said host processor to cause said fan controller to not assert said fault signal upon detection of a fault. However, note that the register disclosed in White does include a "RQST FAIL" bit, (See par. 0079), which is used to enable the indication of a failure of the cooling element.

Beeghly teaches a device comprising a cooling system, (see col. 1, lines 44-47), wherein a disable signal is output in order to prevent a fault signal from being asserted.

Nair, Sekiguchi, White and Beeghly are analogous art because they are all from the same problem solving area, viz., computing devices comprising cooling system control.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the disable signal, taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to provide a bit within said register that would disable the assertion of a fault signal from a fan controller.

One of ordinary skill in the art would have been motivated to combine the teachings because both White and Beeghly disclose that there are conditions in fault recognition systems wherein it is undesirable to assert a fault signal, (see White, par. 0079, and Beeghly, col. 2, lines 42-47). White shows that a fan unit can be disabled from asserting a fault signal that would turn on a visual fault indicator, but Beeghly shows that a fault signal should be disabled from being asserted during certain system conditions wherein such a fault signal could have been asserted erroneously, such as during system start-up. Therefore, one of ordinary skill in the

art would have been motivated to combine fault signal disabling, as taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to prevent asserting a possibly erroneous fault signal during system conditions such as system start-up.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nair, in view of Sekiguchi, as applied to claim 10 above, and further in view of White and Beeghly.

Nair, in view of Sekiguchi, fails to teach that each fan controller includes a register, which said host processor can access to determine which fan controller asserted said fault signal. However, it has been shown that Nair teaches a register included with each fan controller, and also, note Nair, col. 4, lines 1-6, wherein each fan controller includes non-volatile memory for storing alarm information.

White teaches a computer system comprising a cooling fan, in which a fan unit comprises a register, (see par. 0077), which the host processor can access to determine whether the fan unit has assert a fault signal, (see par. 0082, and note lines 4-6).

Nair, in view of Sekiguchi and White, fails to disclose that said register also includes bits which can be set by said host processor to cause said fan controller to not

assert said fault signal upon detection of a fault. However, note that the register disclosed in White does include a "RQST FAIL" bit, (See par. 0079), which is used to enable the indication of a failure of the cooling element.

Beeghly teaches a device comprising a cooling system, (see col. 1, lines 44-47), wherein a disable signal is output in order to prevent a fault signal from being asserted.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to combine the fan unit register field of White, with the fan controller system of Nair, in view of Sekiguchi, in order to improve the host processors ability to monitor the functions of the fan controllers in the event of a cooling system failure.

One of ordinary skill in the art would have been motivated to combine the teachings because the register disclosed in White provides a distinct advantage to the cooling system of Nair, in view of Sekiguchi. Nair teaches that the host processor should have the greatest knowledge of the thermal load of the system, (see col. 3, lines 20-25). As such, one of ordinary skill in the art would have clearly recognized that the host processor must be fully cognizant of the source of any errors encountered in the cooling system. Therefore, there is a clearly represented need for the host processor of Nair to be able to determine the source of a fan fault signal transmitted

in the system of Nair, in view of Sekiguchi. The register of White provides an easily transferable means of utilizing the non-volatile memory, disclosed on col. 4, lines 1-6 of Nair, to provide fault source information to the host processor. One of ordinary skill in the art would have been motivated to combine the register of White with the non-volatile memory of Nair in order to enable host processor access to fault source information.

Moreover, at the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the disable signal, taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to provide a bit within said register that would disable the assertion of a fault signal from a fan controller.

One of ordinary skill in the art would have been motivated to combine the teachings because both White and Beeghly disclose that there are conditions in fault recognition systems wherein it is undesirable to assert a fault signal, (see White, par. 0079, and Beeghly, col. 2, lines 42-47). White shows that a fan unit can be disabled from asserting a fault signal that would turn on a visual fault indicator, but Beeghly shows that a fault signal should be disabled from being asserted during certain system conditions wherein such a fault signal could have been asserted erroneously, such as during system start-up. Therefore, one of ordinary skill in the art would have been motivated to combine fault signal disabling, as taught in Beeghly, with the register of Nair, in view of Sekiguchi and White, in order to prevent

asserting a possibly erroneous fault signal during system conditions such as system start-up.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Schwartz et al, (US 2004/0130868 A1), teaches a cooling system including redundant fan controllers wherein the fan controllers are inter-connected by a fault signal which is used to transmit fault information between the fan controllers without host processor involvement.
- Frankel et al, (US 6,725,132 B2), teaches a cooling system comprising a plurality of fan controllers capable of communicating fault information without host processor involvement, and increasing fan speed to compensate for a failed fan of another controller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron D Matthew whose telephone number is (571) 272-3662. The examiner can normally be reached on Mon-Fri, from 8:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aaron D Matthew
Examiner
Art Unit 2114

ADM

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